This question paper contains 3 printed pages.

6659 *Your Roll No.* .....

B.Sc. (Hons.) (Computer Science) / I Sem. **B**

Paper 104— DIGITAL ELECTRONICS

(Admissions of 2001 and onwards)

Time : 3 hours *Maximum Marks* : 75

(Write your Roll No. on the top immediately on receipt of this question paper.)

Section A is compulsory. Attempt any ***four*** *questions from Section B.*

Section A

1 a) Find the hexadecimal, gray code and excess 3 code equivalents of decimal number 431. (3)

b) Perform the following subtractions using 2s complement arithmetic :-

i) $(256)_{10} - (34)_{10}$

ii) $(-56)_8 - (36)_8$ (2)

2. Simplify the following function in Product of Sum form (use Karnaugh Map)

$F(A,B,C,D) = \sum m(2,3,6,7,8,9,12,13) + \sum d(4,10,14)$ (5)

3. Implement the following function using 8x1 Multiplexer:

$F(A,B,C,D) = \prod(0,1,3,4,8,9,15)$ (5)

4. Design a code converter that converts a decimal digit from 2421 code to BCD. (5)

5. a) Convert a D flip flop into a JK flip flop. (2)

b) What is race condition of a J-K flip flop? In how many ways can this condition be removed? (3)

6. Design a circuit for synchronous mod-5 counter. (5)

7. a) A 8-bit computer has a main memory with the capacity of 64Kbytes. Calculate the following:

i) How many words are stored in the memory?

ii) What is the highest address in hexadecimal? (2)

Turn over

b) Design a circuit for 3-bit even parity generator. (3)

Section B

8. a) Simplify the following Boolean function using Quine Mc-Clusky method:

$F(A,B,C,D) = \sum m(0,2,3,6,8,10,11,12,13,14) + \sum d(9,15)$

Determine essential prime implicants. (6)

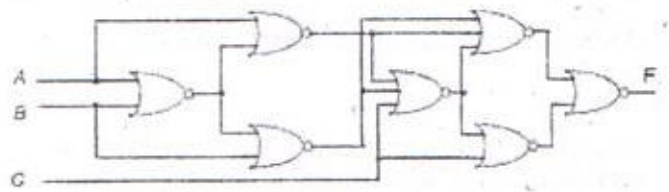
b) Implement the function F with the following two level forms:

$F(A,B,C,D) = \sum(0,1,2,3,4,8,9,12)$

i) NAND-NAND
ii) NAND-AND (4)

9. a) Design a Full Adder using two half Adders. (3)

b) Analyze and determine the function implemented the circuit given below.



(5)

c) Define the fundamental mode operation in asynchronous circuits. (2)

10 a) Given the 8 bit data word 01011011, show the steps to generate the 13 bit composite word for the hamming code that corrects single error and detects double error. (4)

b) Differentiate between a decoder and an encoder. Give the truth table and the circuit for a 4-bit priority encoder. (2+4)

11. a) A sequential circuit has two flip-flops (A and B), one input X, and two outputs Y and Z. The flip-flop input functions and the output functions are:

$JA = B \quad JB = XA' + X'A \quad Y = A' + B$

$KA = XB \quad KB = X' \quad Z = X'B + XA'B'$

Obtain the state equations, the transition (state) table, the transition (state) diagram, and the circuit diagram. (7)

b) Differentiate between synchronous and asynchronous counter. (3)

12. a) For the synchronous sequential circuit described by the following state table, derive the output sequence for the input sequence X = 0010011, assuming that the starting state is:
(i) A (ii) D

Present State	Next State		Output	
	X–0	X–1	X–0	X–1
A	B	C	1	1
B	D	D	1	0
C	B	C	0	1
D	C	A	0	1

(4)

b) A PQ flip flop has 4 operations set 0,1,no change and complement when P and Q inputs are 00,01,10 and 11 respectively. Tabulate its characteristic table and excitation table. Derive its characteristic equation. (4)

c) Draw the logic symbol of a 4kx4 RAM with common input/output pins and an active low chip enable . (2)

13. a) Construct a 32X1 MUX using four 8X1 MUX and a 4X1 MUX. Use block diagrams only.

(4)

b) Give the block diagram for a 3-bit synchronous sequential circuit which has following capabilities:

i) Parallel Load
ii) Right Shift
iii) Left shift

(6)